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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,147	04/27/2005	Susumu Maeda	94198	5289

24628 7590 03/19/2007

WELSH & KATZ, LTD
120 S RIVERSIDE PLAZA
22ND FLOOR
CHICAGO, IL 60606

EXAMINER	
MALEKZADEH, SEYED MASOUD	
ART UNIT	PAPER NUMBER
1722	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,147	MAEDA ET AL.	
	Examiner	Art Unit	
	SEYED MASOUD MALEKZADEH	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/27/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Specification

(b) A brief abstract of the technical disclosure in the specification must commence on a separate sheet, preferably following the claims, under the heading "Abstract" or "Abstract of the Disclosure." The sheet or sheets presenting the abstract may not include other parts of the application or other material. The abstract in an application filed under 35 U.S.C. 111 may not exceed 150 words in length. The purpose of the abstract is to enable the United States Patent and Trademark Office and the public generally to determine quickly from a cursory inspection the nature and gist of the technical disclosure. (See MPEP 608.01(b) [R-3])

The abstract of the disclosure is objected to because the abstract exceeds 150 words in length. Correction is required.

Information Disclosure Statement

An initialed and dated copy of Applicant's IDS form 1449 filed on 04/27/2005 is attached to the instant Office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshi et al. (US 6,565,822) in view of prior art provided by the applicant – Japanese Publication Hiroshi et al (JP 2001-039797).

Hoshi et al ('822) discloses a method of producing a silicon wafer by producing a silicon crystal which the silicon single crystal is grown by the Czochralski method while using and controlling the growth condition of silicon single crystal F/G $[mm^2/°C \div \min]$ (F is the crystal growth rate (mm/min) and G is the temperature gradient [°C./mm] along the crystal growth axis direction in the vicinity of the single crystal growing interface) (See lines 1-9, column 4). In order to produce a silicon wafer not containing defects such as self-interstitial atoms, single crystal growth condition F/G can be controlled by controlling F and G, therefore, such a wafer does not contain I-region (See lines 16-20, column 7). Further, Hoshi et al ('822) teaches producing an epitaxial silicon substrate from a silicon single crystal wafer having no defects such as self-interstitial atoms. (See lines 31-35, column 3). Also, It teaches that if a silicon wafer that does not have defects is used as a substrate of epi-wafer, an epitaxial silicon wafer of high quality will be obtained. (See lines 7-15, column 7). Moreover, Hoshi et al. ('822) teaches an epitaxial growth step of forming the epitaxial growth layer on the silicon wafer substrate. (See lines 43-50, column 3). Furthermore, Hoshi et al. (US '822) further teaches silicon wafer contains boron which during production of silicon single crystal by the Czochralski method, as the boron concentration increases the growth rate decreases. (See lines 23-32, column 2).

Further, Hoshi et al ('822) teaches the temperature of gradient G along the crystal growth axis direction in the vicinity of the single crystal growth interfaces and between a center of the crystal and an edge of the crystal is controlled during the crystal growth in order to produce a silicon wafer which falls out of defect region. (See lines 51-57, column 9 and figure 1)

Furthermore, Hoshi et al ('822) discloses applying a magnetic field during pulling of the silicon crystal production inside of the silicon melt in order to uniform the temperature gradient G in the silicon crystal axis direction uniform between the center of the crystal and the edge of the crystal. (See lines 58-67, column 3 and lines 23-36, column 8)

Moreover, Hoshi et al ('822) discloses in order to control the temperature gradient G in the silicon crystal axis direction to be uniform during silicon crystal production step the silicon crystal is pulled to a magnetic field-free state and then the number of silicon crystal rotation is controlled. (See lines lines 10-24, lines 38-50, column 9 and lines 15-17)

Furthermore, Hoshi et al ('822) discloses a quartz crucible is used to hold the silicon melt during production of silicon crystal.

Further, Hoshi et al ('822) discloses a silicon wafer, which has a size of 100 nm or more and a height of 5 nm or more is used as a silicon wafer for an epitaxial substrate (See lines 17-21, column 3). It further teaches in epitaxial growth step, epitaxial growth layer of the thin film is not more than 2μm on the silicon wafer substrate. (See lines 59-67, column 10 and lines 1-3, column 11)

Furthermore, Hoshi et al ('822) teaches the oxygen concentration of silicon crystal is controlled to be 13 ppma (See lines 3-8, column 12).

Moreover, Hoshi et al ('822) teaches a wafer-like sample sliced from the silicon crystal which its growth condition was controlled to fall within the I-region, then the OSF (oxidation-induced stacking fault) ring was exist inside the I-region which is a defect region. (See lines 58-67, column 11)

Furhtermore, Hoshi et al ('822) also teaches the emergence of the OSF ring also depends on the oxygen concentration in the crystal, and also performing heat treatment. (See lines 1-12, column 12)

However, Hoshi et al. ('822) does not teach the concentration of boron in the silicon crystal.

In the analogous art, Hiroshi et al. (JP 2001-039797) teaches a method of forming an epitaxial layer being a thin film on the surface of silicon crystal, which the thin film is made, by Czochrlski method (CZ process). It further teaches at the time of pull up and growth of the silicon single crystal by CZ method, the concentration of Boron in the silicon crystal is $3\times10^{18} atoms/cm$ or more.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to improve the process of Hoshi et al ('822) by specifying the concentration of boron in the silicon crystal as suggested by Hiroshi et al. (JP '797) in order to control the gettering effect of boron on production of epitaxail wafers.

Remarks

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seyed Masoud Malekzadeh whose telephone number is 571-272-6215. The examiner can normally be reached on Monday – Friday at 8:30 am – 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra N. Gupta can be reached on (571) 272-1316. The fax number for the organization where this application or proceeding is assigned is 571-272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance form a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SMM

ROBERT KUNEMUND
PRIMARY EXAMINER